## AMENDMENTS TO THE CLAIMS

Claims 1-20 are currently pending in the Application. Claims 1, 3, 5-6, 8-11, 13-14, and 17-18 are currently amended to clarify the claimed subject matter(s), without acquiescence in the cited basis for rejections or prejudice to pursue the original claims in a related application. A complete listing of the current pending claims is provided below and supersedes all previous claim listing(s). No new matter has been added.

1. (Currently Amended) A circuit design simulator, comprising:

a stored electronic representation of a circuit design, said circuit design including at least one interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides a digital circuit output and at which said analog circuit receives an input and provides either an output or no output, said digital circuit output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

at least one processor for simulating operation of said circuit design, said at least one processor dynamically determining whether to apply said output or said no output to said node according to said digital circuit output state; and

a storage device configured for storing a result of the simulating operation of said circuit design.

2. (Previously Presented) The circuit design simulator of claim 1, wherein said at least one processor applies said output to said node when said digital circuit output is in said high impedance state, and applies said no output to said node when said digital circuit output is in said digital high state or said digital low state.

3. (Currently Amended) A method for simulating electronic activity at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit provides an output and at which said

analog circuit receives an input, said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

displaying the output on a display apparatus or storing the output in a computer storage device;

using a processor, simulating the circuit design by modeling said output as a digital output signal from said digital circuit to said node when said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when said output is in said high impedance state;

dynamically switching between said digital output signal and said analog output signal based upon whether or not said output is in said high impedance state; and

displaying a result of the act of simulating the circuit design or storing the result in the computer storage device or in a second computer storage device ~~simulation information~~.

4. (Original) The method of claim 3, wherein attributes of said analog output signal are solved for while assuming that no current flows from said digital circuit to said node when said output is in said high impedance state.

5. (Currently Amended) A method for simulating an electronic activity at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a plurality of digital circuits and an analog circuit, said interface comprising a node at which each of said plurality of digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

displaying the output on a display apparatus or storing the output in a computer storage device;

using a processor, simulating the circuit design by modeling at least one of said output as a digital output signal from [[the ]]a corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when ~~said at least one of~~ said output provided by each of said plurality of digital circuits is in said high impedance state;

dynamically switching between said digital output signal and said analog output signal based upon whether or not ~~said at least one of~~ said output provided by each of said plurality of digital circuits is in said high impedance state; and

displaying a result of the act of simulating the circuit design or storing the result ~~simulation information~~ in the computer storage device or in a second computer storage device.

6. (Currently Amended) The method of claim 5, wherein attributes of said analog output signal are solved for while assuming that no current flows from said plurality of digital circuits to said node when ~~said at least one of~~ said output provided by each of said plurality of digital circuits is in said high impedance state.

7. (Previously Presented) The method of claim 5, wherein each said output from said plurality of digital circuits are connected to a bus contention element, said method further comprising collectively resolving each said output from said plurality of digital circuits into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

8. (Currently Amended) A method for simulating electrical operation at an analog/digital interface in a circuit design, said method comprising:

identifying an interface between a digital circuit and an analog circuit, said interface comprising a node at which said digital circuit either outputs a digital signal or else presents a high impedance output so as to be effectively isolated from said node, and at which said analog circuit receives an input signal at an input port;

adding a conditional output signal from said input port of said analog circuit to said node, wherein either an output signal or no output signal is applied from said analog circuit to said node;

using a processor, simulating electrical operation at said interface by applying said output signal from said analog circuit to said node when said digital circuit presents a high impedance output, and applying said no output signal from said analog circuit to said node when said digital circuit presents a digital signal; and

storing simulation information in a computer storage device.

9. (Currently Amended) A computer-readable medium on which is embodied a set of programmed instructions for simulating electronic circuits that cause one or more processors to perform a sequence of steps, said steps comprising:

identifying an interface between one or more digital circuits and an analog circuit, said interface comprising a node at which each of said one or more digital circuits provides an output and at which said analog circuit receives an input, each said output taking on any one of several states including a digital high state, digital low state, or a high impedance state;

displaying the output on a display apparatus or storing the output in a computer storage device;

using a processor, simulating the circuit by modeling at least one of said output provided by said one or more digital circuits as a digital output signal from [[the ]]a corresponding digital circuit to said node when said at least one of said output is not in said high impedance state, and as an analog output signal from said analog circuit to said node when ~~said at least one of~~ said output provided by each of said one or more digital circuits is in said high impedance state; [[and]]

dynamically switching between said digital output signal and said analog output signal based upon whether or not said output provided by each of said one or more digital circuits is in said high impedance state; and

displaying a result of the act of simulating the circuit design or storing the result in the computer storage device or in a second computer storage device ~~simulation information~~.

10. (Currently Amended) The computer-readable medium of claim 9, wherein said programming instructions further cause said one or more processors to perform the step of dynamically switching between said digital output signal and said analog output signal based upon whether or not ~~said at least one of~~ said output provided by each of said one or more digital circuits is in said high impedance state.

11. (Currently Amended) The computer-readable medium of claim 10, wherein said programming instructions further cause said one or more processors to solve for attributes of said analog output signal while assuming that no current flows from said one or more digital circuits to said node when ~~said at least one of~~ said output provided by each of said one or more digital circuits is in said high impedance state.

12. (Previously Presented) The computer-readable medium of claim 10, wherein said one or more digital circuits comprise a plurality of circuits, and each said output from said plurality of circuits is connected to a bus contention element, said programming instructions causing said one or more processors to further perform the step of collectively resolving each said output into a single output signal, said single output signal taking on any one of several states including said digital high state, said digital low state, or said high impedance state.

13. (Currently Amended) A method for simulating a circuit design, comprising the steps of:

identifying an interface between a plurality of digital circuit outputs and an analog circuit input, wherein each of said plurality of digital circuit outputs can present a high impedance state;

modeling said interface by using a processor to add ~~adding~~ an output from an analog circuit receiving said analog circuit input to said interface;

displaying the output on a display apparatus or storing the output in a computer storage device;

using a processor, simulating electrical operation at said modeled interface by resolving an electrical state of said interface using only the output from the analog circuit when all of said plurality of digital circuit outputs are in a high impedance state, and resolving the electrical state of said interface using one or more of said plurality of digital circuit outputs otherwise; and

displaying a result of the act of simulating the circuit design or storing the result in the computer storage device or in a second computer storage device ~~simulation information~~.

14. (Currently Amended) A mixed analog/digital simulator comprising:

a simulation processor;

said simulation processor including a computer-readable medium on which is embodied a set of programmed instructions that cause said simulation processor to simulate an operation of a design circuit, wherein said design circuit includes:

(1) a digital circuit having an output;

(2) a network electrically coupled to said digital circuit output, said network formed by electrically coupling an input of each of a plurality of circuit blocks at a network input node;

(3) said circuit blocks including at least one analog circuit having an analog circuit input electrically coupled to said network input node;

(4) said analog circuit having an input mode of operation for receiving an input signal at said analog circuit input and an output mode of operation for producing an output signal at said analog circuit input;

(5) said digital circuit output being applied to said network input node when said digital circuit is in a non-high-impedance state; and

(6) said output signal of said analog circuit being applied to said network input node when said digital circuit is in a high-impedance state; and

a tangible computer accessible medium or a storage device configured for storing a result of simulating an operation of a design circuit by the simulation processor or a display apparatus configured for displaying the result.

15. (Previously Presented) The simulator of claim 14, wherein said output signal of said analog circuit is operably coupled to a plurality of digital circuit outputs using a bus.

16. (Previously Presented) The simulator of claim 14, wherein said input mode and output mode are selected automatically and dynamically according to a state of said digital circuit.

17. (Currently Amended) A method of simulating a mixed analog/digital system ~~systems~~, comprising:

transforming an input of an analog circuit into an ioput, said ioput having a conditional output feeding back to a bus, said ioput being operable under a high-impedance input state, and said ioput capable of accepting a digital signal input and producing an analog signal output;

displaying said digital signal input, said analog signal output, or said ioput on a display apparatus or storing said digital signal input, said analog signal output, or said ioput in a computer storage device;

electrically coupling said ioput to a digital circuit output and to inputs of a plurality of additional circuits;

receiving said digital signal input at said ioput when said digital circuit output is in a non-high-impedance state;

applying said analog signal output at said ioput when said digital circuit output is in a high-impedance state; and

using a processor, simulating the mixed analog/digital system by solving the mixed analog/digital system ~~systems~~ for simulation information based upon at least a result of the act of receiving said digital signal input or the act of applying said analog signal output and storing the simulation information in the computer storage device or in a second computer storage device.

18. (Currently Amended) The method of claim 17, wherein said act of electrically coupling comprises coupling said ioput to a plurality of digital circuit outputs using a bus.

19. (Previously Presented) The method of claim 3, further comprising:

providing the input received by the analog circuit in the form of an analog tri-statable ioput, wherein the analog tri-statable ioput drives a non-Z value using an output portion, and all other digital drivers are driving a Z value.

20. (Previously Presented) The method of claim 19, further comprising:

receiving, as the ioput, an output non-Z signal using an input portion, wherein one or more of the all other digital drivers are driving a non-Z signal using the output portion.